REMARKS

Reconsideration of this application, as amended, is respectfully requested.

Claims 1-14 are pending. Claims 1-14 stand rejected. Claims 1 and 13 have been objected to.

Claims 1 and 13 have been amended. Claim 7 has been canceled. Support for the amendments is found in the specification, the drawings, and in the claims as originally filed. Applicants submit that the amendments do not add new matter.

Claim Rejections - 35 U.S.C. §§ 102/103

Claims 1, 8, 9 and 12 stand rejected under 35 U.S.C. §102(b) as being anticipated by U.S. Patent No. 5,041,885 of Gualandris, et al. ("Gualandris"). Claim 2 stands rejected under 35 U.S.C. §103 as being unpatentable over U.S. Patent No. 5,041,885 of Gualandris, et al. ("Gualandris") as applied to claims 1, 8, 9 and 12 above, and further in view of U.S. Patent No. 5,970,351 of Takeuchi ("Takeuchi"). Claim 3 stands rejected under 35 U.S.C. §103 as being unpatentable over U.S. Patent No. 5,041,885 of Gualandris, et al. ("Gualandris") as applied to claims 1, 8, 9 and 12 above, and further in view of U.S. Patent No. 6,057,582 of Choi ("Choi_1"). Claim 4 stands rejected under 35 U.S.C. §103 (a) as being unpatentable over U.S. Patent No. 5,041,885 of Gualandris, et al. ("Gualandris") in view of Takeuchi " 351 as applied to claim 2 above, and further in view of U.S. Patent No. 6,057,582 of Choi ("Choi_1"). Claims 5 and 6 stand rejected under 35 U.S.C. §103 as being unpatentable over U.S. Patent No. 5,041,885 of Gualandris, et al. ("Gualandris") as applied to claims 1, 8, 9 and 12 above, and further in view of U.S. Patent No. 5, 793,088 of Choi ("Choi_2"). Claims 7, 10 and 11 stand rejected under 35 U.S.C. §103 as being unpatentable over U.S. Patent No. 5,041,885 of Gualandris, et al. ("Gualandris") in view of U.S. Patent No. 5,824,587 of Krivokapic ("Krivokapic"). Claim 13 stands rejected under 35 U.S.C. §103 as being unpatentable over U.S. Patent No. 5,041,885 of Gualandris, et al. ("Gualandris") in view of

U.S. Patent No. 6,274,894 B1 of Wieczorek, et al. ("Wieczorek") and further in view of U.S. Patent No. 5,970,351 of Takeuchi ("Takeuchi"). Claim 14 stands rejected under 35 U.S.C. §103 as being unpatentable over U.S. Patent No. 5,041,885 of Gualandris, et al. ("Gualandris") in view of U.S. Patent No. 6,274,894 B1 of Wieczorek, et al. ("Wieczorek") and further in view of U.S. Patent No. 5,970,351 of Takeuchi ("Takeuchi") and applied to claim 13 above, and further in view of U.S. Patent No. 6,057,582 of Choi ("Choi"). The Examiner stated that

> Gualandris discloses (see, for example, Fig. 4) a field effect transistor (device) comprising a gate oxide (gate dielectric) 2, silicon substrate having an electrical semiconductivity of a first type (first conductivity region of a substrate) 5, gate electrode 1, oxide spacers (pair of sidewall spacers) 6, and source and drain regions of a polarity opposite to the polarity of the silicon substrate (a pair of silicon or silicon alloy inwardly concaved source/drain region of a second conductivity type formed in said substrate) 7. The source and drain regions 7 are inwardly concaved and bed (inflection points) directly underneath the gate electrodel. The channel region 5 directly beneath the gate electrode is larger than the channel region between the inflection points.

(p. 2, Office Action 2/17/04)

In particular, with respect to claim 7, the Examiner stated that

> Gualandris does not disclose an inflection point which occurs between 50-200 A laterally beneath said gate electrode and at a depth of between 12-200 A beneath said gate dielectric. However, it would have been obvious to one of ordinary skill in the art at the time of invention was made to use these depths in order to form an adequate channel underneath the gate electrode, and since it has been held that where the general conditions of a claim are disclosed in the prior art, discovering the optimum or working ranges involves only routine skill in the art.

(p. 5, Office Action 2/17/04)

Applicants respectfully disagree. It is Applicants' understanding that the cited references fail to teach or render obvious Applicants' invention as set forth in claims 1-14. Applicants have amended claims 1 and 13 and canceled claim 7 to more particularly point out and distinctly claim the subject matter, which Applicants regard as the invention. More specifically, Applicants have amended claim 1 to indicate that a pair of silicon or silicon alloy

inwardly concaved source/drain regions of the presently claimed invention have inflection points directly beneath a lower portion of the gate electrode and extend the greatest distance laterally beneath the lower portion of the gate electrode at the inflection points between 50-250Å laterally beneath the gate electrode and at a depth of between 25-200Å beneath the gate dielectric.

Amended claim 1 reads as following:

> A device comprising:
>
> a gate dielectric formed on first conductivity region of a substrate;
>
> a gate electrode formed on said gate dielectric, said gate electrode having a lower portion formed directly on said gate dielectric;
>
> a pair of silicon or silicon alloy inwardly concaved source/drain regions of a second conductivity type formed in said substrate and on opposite sides of said gate electrode and creating inflection points directly beneath said lower portion of said gate electrode formed directly on said gate dielectric layer, wherein said silicon or silicon alloy source/drain regions extend the greatest distance laterally beneath said lower portion of the gate electrode at said inflection points which occurs between 50-250Å laterally beneath said gate electrode and at a depth of between 25-200Å beneath said gate dielectric and define a channel region directly beneath said lower portion of said gate electrode in said first conductivity type region, and wherein said channel region directly beneath said lower portion of said gate electrode is larger than said channel region between said inflection points.

(Amended claim 1) (emphasis added)

In contrast to the presently claimed invention, Gualandris discloses a surface field effect transistor with depressed source and/or drain areas for ULSI integrated devices.

Gualandris discloses that

> A surface field effect integrated transistor has the surface of the silicon in the source and drain areas lowered by 50-500nm in respect to the surface of the silicon underneath the gate electrode by etching the silicon substrate before forming the source and drain junctions. The transistor is sturdy and reliable because of the backing-off of the multiplication zone of the charge carriers from the gate oxide by a distance greater than several times the mean free path of hot carriers, thus markedly reducing the number of hot carriers available for injection in the gate oxide.

(Gualandris, Abstract)(emphasis added)

More significantly, Gualandris discloses

> In accordance with the present invention this objective is reached by means of a novel surface field effect transistor structure wherein, at least in an area corresponding to the drain region of the transistor, the surface of the semiconducting substrate is depressed relatively to the level of the surface of the semiconducting substrate in the respective gate area of the transistor. This may be obtained by etching the monocrystalline silicon commonly constituting the semiconducting substrate in the drain area in order to lower the level of the surface of the substrate by a depth of between about 50 and about 500nanometers (nm). Below 50 nm the beneficial effects are substantially lost while above 500nm an excessive reduction of the gain may also be observed.

(Gualandris, col.2, lines 49-63) (emphasis added)

Thus, Gualandris merely discloses etching the surface of the silicon substrate by a depth of between about 50nm (i.e. 500 Å) and about 500 nm (i.e. 5000 Å) to lower the source and drain regions in respect to the surface of the silicon underneath the gate electrode to "decouple" the source/drain junctions from the channel region of the transistor and does not disclose a pair of silicon or silicon alloy inwardly concaved source/drain regions that have inflection points directly beneath a lower portion of the gate electrode and extend the greatest distance laterally beneath the lower portion of the gate electrode at the inflection points between 50-250Å laterally beneath the gate electrode and at a depth of between 25-200Å beneath the gate dielectric, as recited in amended claim 1.

Furthermore, Applicants respectfully submit that Gualandris, in contrast to the Examiner's assertion, teaches away from the presently claimed invention by stating that for lowering the surface of the silicon in the source and drain areas by less than 50nm-500nm (i.e. 500 Å to 5000 Å) to the surface of the silicon underneath the gate electrode, "the beneficial effects [of the invention] are substantially lost".

Because Gualandris does not set forth all the limitations of amended claim 1, applicants respectfully submit that amended claim 1 is not anticipated by Gualandris under 35 U.S.C. 102§(b).

Given that dependent claims 8, 9, and 12 depend directly on claim 1 and contain at least the same limitations as amended claim 1, applicants respectfully submit that claims 8, 9, and 12 are likewise not anticipated by Gualandris under 35 U.S.C. §102(b).

Takeuchi, in contrast to the presently claimed invention, discloses a method of producing a transistor with a source and drain diffusion layer having a shallow junction depth that results in a low parasitic resistance and a low parasitic capacitance of the transistor. According to Takeuchi, the shallow junction depth of the source and drain regions is achieved by selectively growing a thin semiconductor film of the appropriate conductivity type on the surface of the substrate to form elevated source and drain regions. More specifically, Takeuchi discloses, for example, in the case of an n-type silicon substrate:

> Then, a silicon single crystal thin film doped with boron to the order of 10^19 to 10^20 atoms/cm^3 is selectively grown only at the exposed portion of the surface of the substrate to form elevated source and drain 7, FIG. 4 (b). The growth is performed at a temperature as low as possible (for example, 600C.), so that boron is not diffused into the substrate during the growth making the transition of the concentration at the boundary between elevated source and drain 7 and the silicon substrate steep like a staircase.

(Takeuchi, col.7, lines 46-54) (emphasis added)

Further, Takeuchi discloses:

> Thereafter, annealing is performed so that the boron contained in elevated source and drain 7 is diffused into silicon substrate 1 to form source and drain junction surface 9 in the inside of the substrate. This annealing is performed to such a degree that source and drain junction surface 9 reaches just below gate electrode 4 (FIG. 4(c)). Accordingly, the depth of the junction can be suppressed to a degree equal to the thickness of sidewall insulator 6.

(Takeuchi, col.8, lines 16-25) (emphasis added)

Moreover, Takeuchi discloses that

> It is to be noted that, if the last-mentioned annealing is omitted, then a MOSFET having a junction depth close to the ideal junction depth of zero can be realized.

(Takeuchi, col.8, lines 26-28) (emphasis added)

Thus, Takeuchi discloses elevated drain/source regions of the transistor formed from a thin semiconductor film layer of the appropriate conductivity type on the surface of the substrate with the source and drain junctions having minimal extensions into the substrate, and accordingly, just beneath the vertical sidewall isolators of the gate electrode, aiming at the ideal junction depth of zero. In contrast to the presently claimed invention, Takeuchi does not disclose, teach or suggest a pair of silicon or silicon alloy inwardly concaved source/drain regions having inflection points directly beneath a lower portion of the gate electrode and extending the greatest distance laterally beneath the lower portion of the gate electrode at the inflection points between 50-250Å laterally beneath the gate electrode and at a depth of between 25-200Å beneath the gate dielectric.

Choi_1 discloses a semiconductor device in which a gate insulating film is formed thicker at portions opposite to the edge portions of a gate electrode for preventing the hot carrier to occur due to a strong electric field of the gate electrode. More specifically, Choi_1 discloses the formation of the gate electrode as following:

> Then, as shown in FIG. 4C, the exposed edge portion of the gate electrode 23a is etched to a depth using the photoresist film 24a as a mask. And, n- impurities are injected using the gate electrode 23a as mask, to form LDD regions 25 in surfaces of the semiconductor substrate 21 on both sides of the gate electrode 23a. Then, as shown in FIG. 4D, after removing the photoresist film 24a, an oxidation process is conducted to bend the edge portion of the gate electrode 23a having an etched portion upward. This is possible because the oxidation is more active at the edge portion of the gate insulating film 22 in the oxidation process due to the thin gate electrode 23a having an etched portion formed thicker than other regions. After completion of the oxidation process, an insulating film is formed on an entire surface of the semiconductor substrate 21 inclusive of the gate electrode 23a and etched back, to form insulating sidewalls 26 at both sides of the gate electrode 23a. Thereafter, upon making a heavy injection of n+ impurities using the gate electrode 23a and the insulating sidewalls 26 as masks, source and drain impurity regions 27 are formed in surfaces of the semiconductor substrate 21 on both sides of the gate electrodes 23a.

(Choi, col. 4, lines 17-39)(emphasis added)

In contrast to the presently claimed invention, Choi_1 merely discloses a transistor having the gate electrode with center portions formed thicker than the end portions and drain/source regions generated by injecting n-impurities using the gate electrode as a mask to form source/drain (LDD) regions on both sides, and not underneath, the gate electrode. Thus, Choi_1 also does not disclose, teach, or suggest a pair of silicon or silicon alloy inwardly concaved source/drain regions having inflection points directly beneath a lower portion of the gate electrode and extending the greatest distance laterally beneath the lower portion of the gate electrode at the inflection points between 50-250Å laterally beneath the gate electrode and at a depth of between 25-200Å beneath the gate dielectric, as recited in amended claim 1.

Choi_2 discloses a method and structure for controlling threshold voltage of MOSFET. The method compensates for the edge effect associated with halo implants by utilizing an edge threshold implant (VT implant), which passes impurities through dielectric spacers, through the underlying source/drain regions and into the edges of the halo regions which lie in the channel, reducing junction capacitance without degradation of punch-through voltage. More specifically, referring to Figure 2, Choi_2 discloses:

> Structure 106 includes a silicon substrate 108 having p-well 110. P-well 110 has formed therein p-type halo regions 120, 122, n-type source/drain regions 126, 128, 130, 132 and p-type channel 112. In particular, n-type source/drain regions 126, 130 and 128, 132 are formed within p-type halo regions 120, 122, respectively. Further, n-type source/drain regions 126, 128 underlie dielectric spacers 134, 136, respectively, and n-type source/drain regions 130, 132 are laterally separated from gate 119 by dielectric spacers 134, 136, i.e. do not underlie gate 119.

(Choi_2, col. 5, lines 30-39).

In contrast to the presently claimed invention, Choi_2 merely discloses compensation for the high dopant concentrations of the portions of the halo regions located at the edges of the transistor channel by doping with VT implants and source/drain regions created by injecting n-impurities using the gate electrode as a mask to form source/drain (LDD) regions

on both sides of the gate electrode, underneath isolating sidewalls, and not underneath the gate electrode. Accordingly, Choi_2 also fails to disclose, teach, or suggest a pair of silicon or silicon alloy inwardly concaved source/drain regions having inflection points directly beneath a lower portion of the gate electrode and extending the greatest distance laterally beneath the lower portion of the gate electrode at the inflection points between 50-250Å laterally beneath the gate electrode and at a depth of between 25-200Å beneath the gate dielectric, as recited in amended claim 1.

Krivokapic discloses a method for making a convex device with an elevated gate structure. More specifically, Krivokapic discloses

> As shown in FIG. 2 (p), the completed transistor is formed on a convex substrate surface with the base of the gate 210 being elevated above source 217 and drain 218. The gate structure resides above the highest region of the convex substrate surface and is separated from the substrate surface by the gate oxide 208. The gate structure extends laterally above the substrate surface until the substrate surface begins to slope downward. Underlying the downward sloping convex regions of the substrate surface are the source 217 and drain 218.

(Krivokapic, col.9, lines 41-50) (emphasis added)

In contrast to the presently claimed invention, Krivokapic discloses the source and drain that underlie merely the downward sloping convex region of the substrate surface and not the gate structure that is located above the flat center portion of the substrate surface before it begins to slope downward and also fails to disclose, teach, or suggest a pair of silicon or silicon alloy inwardly concaved source/drain regions having inflection points directly beneath a lower portion of the gate electrode and extending the greatest distance laterally beneath the lower portion of the gate electrode at the inflection points between 50-250Å laterally beneath the gate electrode and at a depth of between 25-200Å beneath the gate dielectric, as recited in amended claim 1.

Hence, none of Gualandris, Takeuchi, Choi_1, Choi_2, or Krivokapic disclose, teach, or suggest a pair of silicon or silicon alloy inwardly concaved source/drain regions having inflection points directly beneath a lower portion of the gate electrode and extending the greatest distance laterally beneath the lower portion of the gate electrode at the inflection points between 50-250Å laterally beneath the gate electrode and at a depth of between 25-200Å beneath the gate dielectric, as recited in amended claim 1.

Consequently, even if Gualandris, Takeuchi, Choi_1, Choi_2, and Krivokapic were combined, such a combination would lack the limitation of claim 1 of a pair of silicon or silicon alloy inwardly concaved source/drain regions having inflection points directly beneath a lower portion of the gate electrode and extending the greatest distance laterally beneath the lower portion of the gate electrode at the inflection points between 50-250Å laterally beneath the gate electrode and at a depth of between 25-200Å beneath the gate dielectric.

Therefore, applicants respectfully submit that amended claim 1 is not obvious under 35 U.S.C. § 103 (a) over Gualandris, in view of Takeuchi and further in view of Choi_1, Choi_2, and Krivokapic.

Given that claims 2-6 and 8-12 depend on claim 1, either directly or indirectly, and add additional limitations, applicants submit that claims 2-6 and 8-12 are not obvious under 35 U.S.C. §103 (a) over Gualandris, in view of Takeuchi and further in view of Choi_1, Choi_2, and Krivokapic.

Additionally, with respect to claim 13, Wieczorek discloses a transistor with source and drain regions having lower-bandgap portions that underlie sidewall spacers of the gate electrode and not the gate electrode itself (see, for example, Fig. 10). Moreover, citing prior art, Wieczorek points out that extending the source/drain regions underneath the gate electrode is undesirable. More specifically, Wieczorek discloses that

> A more realistic representation of a MOSFET with LDD regions is shown in FIG. 2. The transistor of FIG. 2 differs from that of FIG. 1 in that LDD portions 18 are partially below gate conductor 14, rather than being aligned under spacers 16. In addition, source/drain portions 20 are partially below spacers 16, rather than being aligned outside of spacers 16. This change in the position of portions 18 and 20 from the as-implanted distributions is a result of diffusion of the implanted impurities during the subsequent fabrication steps. The speed and extent of this diffusion is enhanced by the presence of structural defects introduced into substrate 10 during ion implantation of portions 18 and 20. Such defect-enhanced diffusion is also referred to as "transient-enhanced diffusion" (TED), wherein defects or other incidences of nonuniform structure (such as doping nonuniformities) are termed "transients". The movement of source/drain portions 18 and 20 undesirably decreases the effective length of the channel to a value smaller than that defined by the length of gate conductor 14. Furthermore, the defect-enhanced diffusion of portions 18 and 20 may not occur in a reliable, repeatable way, making predictable device fabrication difficult.

(Wieczorek, col. 2, lines 8-30)

In addition, in the part of the reference cited by the Examiner, Wieczorek merely discloses using advantages of SiGe as a low-band gap material to form a part of the drain/source region of the transistor.

Thus, in contrast to the presently claimed invention, Wieczorek also fails to disclose, teach, or suggest a pair of silicon-germanium alloy inwardly concaved source/drain regions having inflection points directly beneath a lower portion of the gate electrode and extending the greatest distance laterally beneath the lower portion of the gate electrode at the inflection points between 50-250Å laterally beneath the gate electrode and at a depth of between 25-200Å beneath the gate dielectric, as recited in amended claim 13:

> A device comprising:
>
> a gate dielectric formed on a first conductivity type region of a substrate;
>
> a gate electrode formed on said gate dielectric, said gate electrode having a lower portion formed directly on said gate dielectric;
>
> a pair of sidewall spacers formed along laterally opposite sidewalls of said gate electrode; and
>
> a pair of silicon-germanium alloy source/drain regions having a second conductivity type formed in said substrate and along opposite sides of said gate electrode wherein said silicon-germanium alloy source/drain regions in said substrate are inwardly concaved and create an inflection point in said substrate directly beneath said lower portion of said gate electrode formed directly on said gate dielectric,

wherein said silicon-germanium alloy source/drain regions extend the greatest distance laterally beneath said gate electrode at said inflection points which occurs between 50-250Å laterally beneath said gate electrode and at a depth of between 25-200Å beneath said gate dielectric, said silicon germanium alloy extends above the height of said gate dielectric layer wherein the top surface of said deposited silicon-germanium alloy is spaced further from said gate electrode than said silicon-germanium alloy adjacent to said gate dielectric.

(Amended claim 13)(emphasis added)

Accordingly, as set forth herein, none of the references mentioned above disclose, teach, or suggest a pair of silicon-germanium alloy inwardly concaved source/drain regions having inflection points directly beneath a lower portion of the gate electrode and extending the greatest distance laterally beneath the lower portion of the gate electrode at the inflection points between 50-250Å laterally beneath the gate electrode and at a depth of between 25-200Å beneath the gate dielectric, as recited in amended claim 13.

Consequently, even if the all the references mentioned above were combined, such a combination would lack the limitation of claim 13 of a pair of silicon or silicon alloy inwardly concaved source/drain regions having inflection points directly beneath a lower portion of the gate electrode and extending the greatest distance laterally beneath the lower portion of the gate electrode at the inflection points between 50-250Å laterally beneath the gate electrode and at a depth of between 25-200Å beneath the gate dielectric.

Therefore, applicants respectfully submit that amended claim 13 is not obvious under 35 U.S.C. § 103 (a) over all references mentioned above.

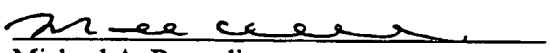
Given that claim 14 depends on claim 13, and adds additional limitations, applicants submit that claim 14 is not obvious under 35 U.S.C. §103 (a) over all above mentioned references as well.

It is respectfully submitted that in view of the amendments and arguments set forth herein, the applicable rejections and objections have been overcome. If there are any additional charges, please charge Deposit Account No. 02-2666 for any fee deficiency that may be due.

Respectfully submitted,

BLAKELY, SOKOLOFF, TAYLOR & ZAFMAN

Date: 4/21/04



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